

256K (32K x 8) Static RAM

Features

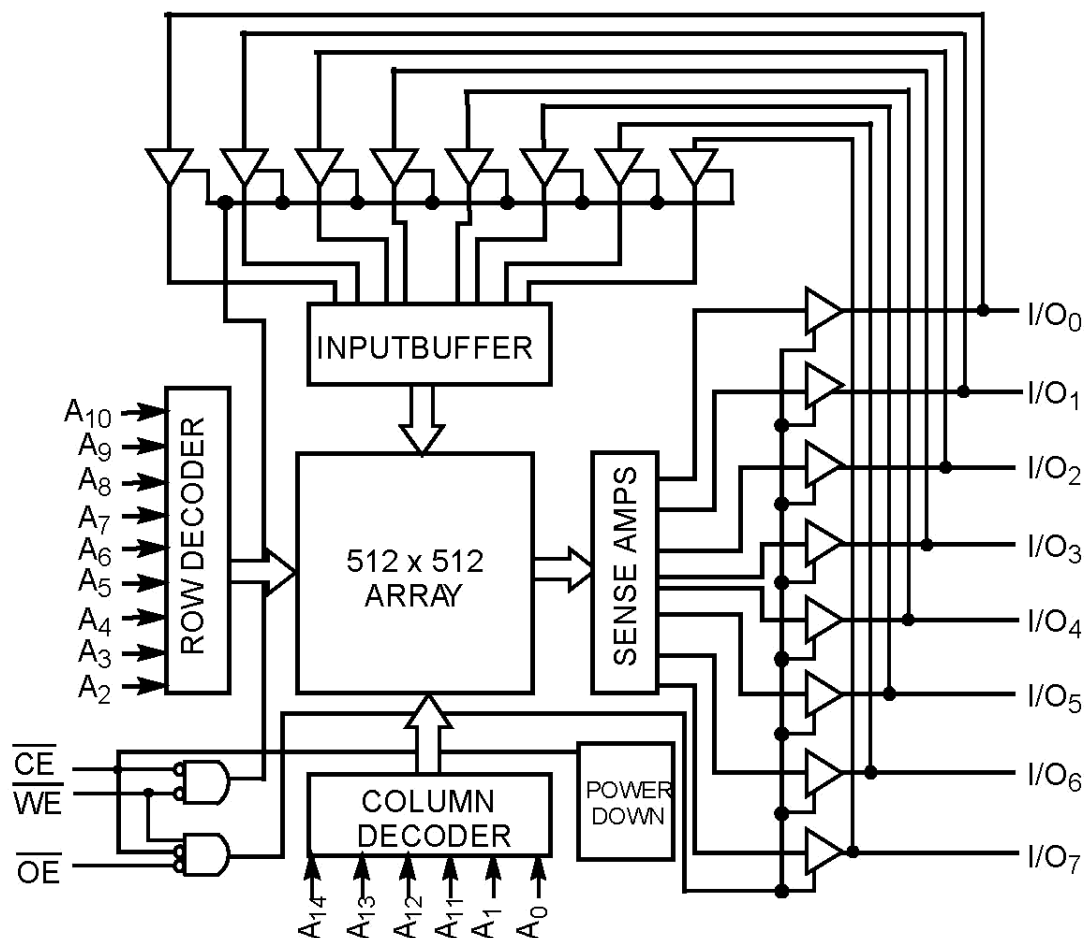
- Temperature Ranges
 - Commercial: 0 to 70
 - Industrial: -40 to 85
 - Automotive: -40 to 125
- High speed: 55ns and 70 ns
- Voltage range : 4.5V –5.5V operation
- Low active power (70ns, LL version, Com'l and Ind'l)
 - 275mW (max)
- Low standby power (70ns, LL Version, Com'l and Ind'l)
 - 28 μ W (max.)
- Easy memory expansion with $\overline{CS}$ and $\overline{OE}$ features
- TTL – compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Package available in a standard 450-mil-wide (300-mil body width) 28-lead narrow SOIC, 28-lead TSOP-1, 28-lead reverse TSOP-1, and 600-mil 28-lead PDIP packages.

Functional Description [1]

The CY62256 is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW output enable ($\overline{OE}$) and active LOW output enable ($\overline{OE}$) and three-state drives. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected.

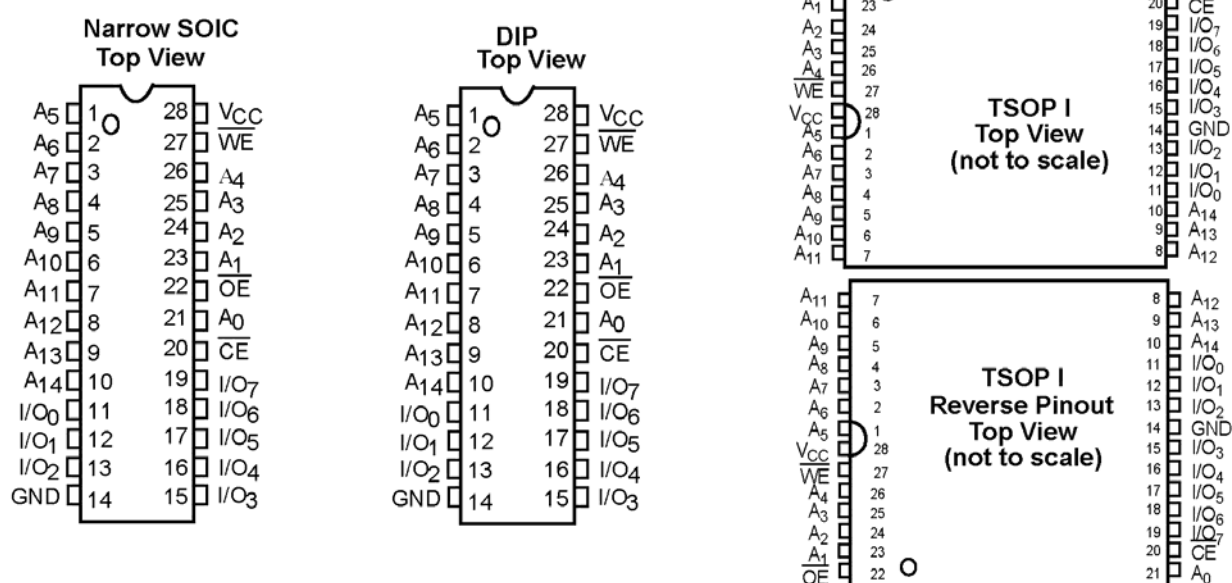
An active Low write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins. The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Product Portfolio

Product		Vcc Range (V)			Speed (ns)	Power Dissipation			
		Min.	Typ.[2]	Max.		Operating, Icc (mA)		Standby, ISB2(μA)	
						Typ.[2]	Max.	Typ.[2]	Max.
CY62256	Commercial	4.5	5.0	5.5	70	28	55	1	5
CY62256L	Com'l / Ind'l				55/70	25	50	2	50
CY62256LL	Commercial				70	25	50	0.1	5
CY62256LL	Industrial				55/70	25	50	0.1	10
CY62256LL	Automotive				55	25	50	0.1	15

Pin Configurations

Pin Definitions

Pin Number	Type	Description
1-10,21,23-26	Input	A ₀ -A ₁₄ . Address Inputs
11-13,15-19,	Input/Output	I/O ₀ -I/O ₇ . Data lines. Used as input or output lines depending on operation
27	Input/Control	$\overline{WE}$. When selected Low, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	$\overline{CE}$. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	$\overline{OE}$. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins
14	Ground	GND. Ground for the device
28	Power Supply	V _{cc} . Power supply for the device

Notes:

2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A = 25^\circ\text{C}$, V_{cc}). Parameters are guaranteed by design and characterization, and not 100% tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....-65 to +150

Ambient Temperature with

Power Applied.....-55 to +125

Supply Voltage to Ground Potential

(Pin 28 to Pin 14).....-0.5V to +7.0V

DC Voltage Applied to Outputs

In High-Z State ^[3].....-0.5V to V_{CC} +0.5V

DC Input Voltage ^[3].....-0.5V to V_{CC} +0.5V

Output Current into Outputs (LOW).....20mA

Static Discharge Voltage.....>2001V

(per MIL-STD-883, Method 3015)

Latch-up Current.....>200mA

Operating Range

Range	Ambient Temperature(T _A) ^[4]	V _{CC}
Commercial	0 to +70	5V ± 10%
Industrial	-40 to +80	5V ± 10%
Automotive	-40 to +125	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256-55			CY62256-70			Unit
			Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-1.0mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =2.1mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} +0.5V	2.2		V _{CC} +0.5V	V
V _{IL}	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V
I _{LX}	Output Leakage Current	GND ≤ V _I ≤ V _{CC}	-0.5		+0.5	-0.5		+0.5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-0.5		+0.5	-0.5		+0.5	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0mA, f=f _{MAX} = 1/t _{RC}		28	55		28	55	mA
		L		25	50		25	50	mA
		LL		25	50		25	50	mA
I _{SB1}	Automatic CE Power-down Current-TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IH} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f=f _{MAX}		0.5	2		0.5	2	mA
		L		0.4	0.6		0.4	0.6	mA
		LL		0.3	0.5		0.3	0.5	mA
I _{SB2}	Automatic CE Power-down Current-CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC}-0.3V$, V _{IN} ≥ V _{CC} -0.3V, or V _{IN} ≤ 0.3V, f=0		1	5		1	5	mA
		L		2	50		2	50	μA
		LL		0.1	5		0.1	5	μA
		LL-Ind'l		0.1	10		0.1	10	μA
		LL-Auto		0.1	15				μA

Capacitance ^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A =25 , f=1MHz	6	pF
C _{OUT}	Output Capacitance	V _{CC} =5.0V	8	pF

Notes:

3.V_{IL} (min.)=-2.0V for pulse durations of less than 20ns.

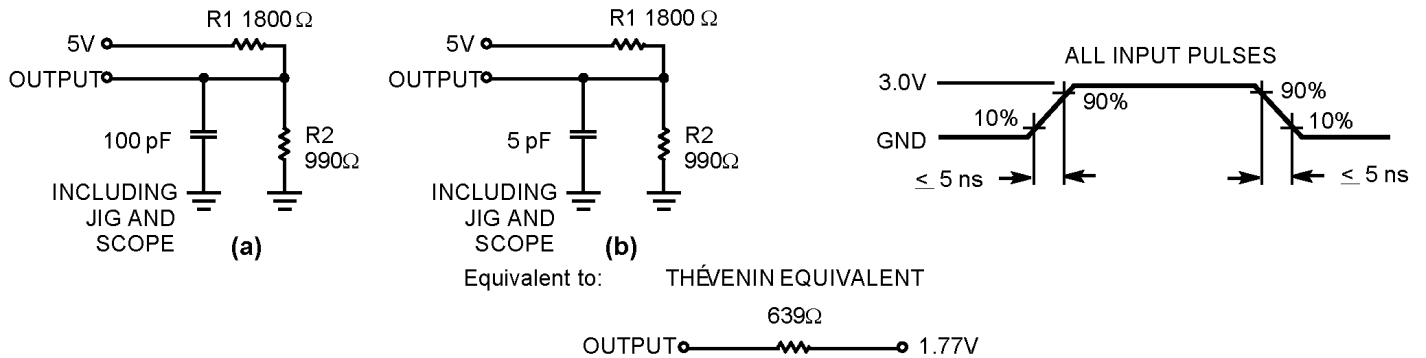
4.T_A is the "Instant-On" case temperature.

5.Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Description	Test Conditions	Symbol	DIP	SOIC	TSOP	RTSOP	Unit
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 Inch, 4-layer printed circuit board	Θ_{JA}	75.61	76.56	93.89	93.89	/W
Thermal Resistance (Junction to Case) ^[5]		Θ_{JC}	43.12	36.07	24.64	24.64	/W

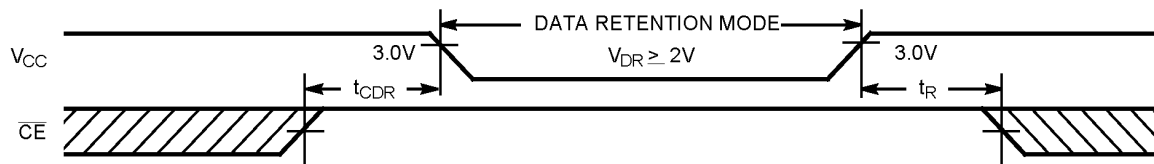
AC Test Loads and Waveforms



Data Retention Characteristics

Parameter	Description	Conditions[5]	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}	Data Retention Current	L	$V_{CC}=3.0V, \overline{CE} \geq V_{CC}-0.3V,$ $V_{IN} \geq V_{CC}-0.3V, \text{ or } V_{IN} \leq 0.3V$	2	50	μA
		LL		0.1	5	μA
		LL-Ind'l		0.1	10	μA
		LL-Auto		0.1	10	μA
$t_{CDR}[5]$	Chip Deselect to Data Retention Time		0			ns
$t_R[5]$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform

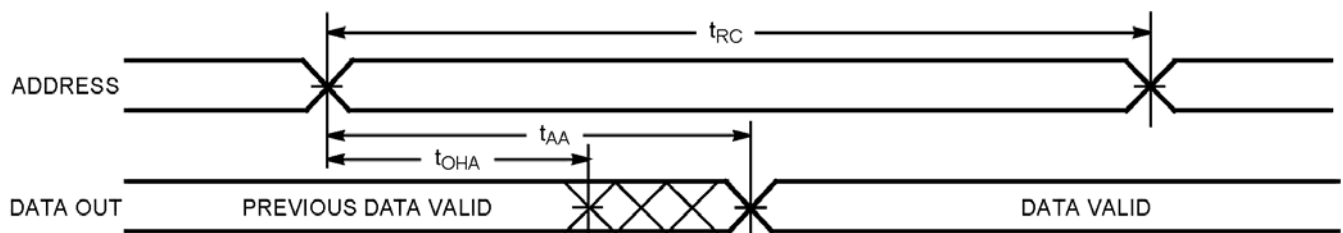


Notes:

6. No input may exceed $V_{CC} + 0.5$.

Switching Characteristics Over the Operating Range ^[7]

Parameter	Description	Cy62256-55		CY62256-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	$\overline{OE}$ LOW to Data valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[8]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[8,9]		20		25	ns
t _{LZOE}	$\overline{OE}$ LOW to LOW-Z ^[8]	5		5		ns
t _{HZCE}	$\overline{OE}$ LOW to LOW-Z ^[8,9]		20		25	ns
t _{PU}	$\overline{OE}$ LOW to Power-up	0		0		ns
t _{PD}	$\overline{OE}$ HIGH to Power-down		55		70	ns
Write Cycle ^[10,11]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{OE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t _{SD}	Data Set-up to write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[8,9]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[8]	5		5		ns

Switching Waveforms
Read Cycle NO. 1 ^[12,13]

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference level is of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.

8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZOE} , and t_{HZOE} is less than t_{HZCE} , and t_{LZWE} for any given device.

9. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L=5pF$ as in (b) of AC Test Loads. Transition is measured $\pm 500mV$ from steady-state voltage.

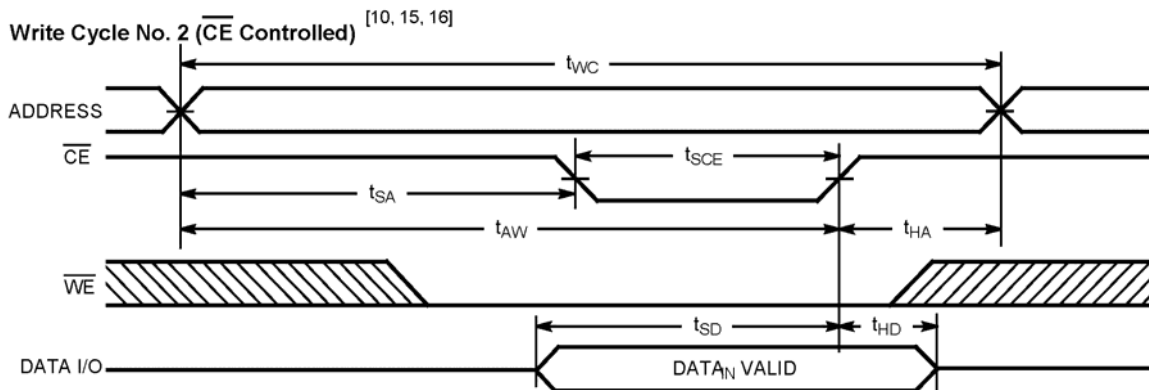
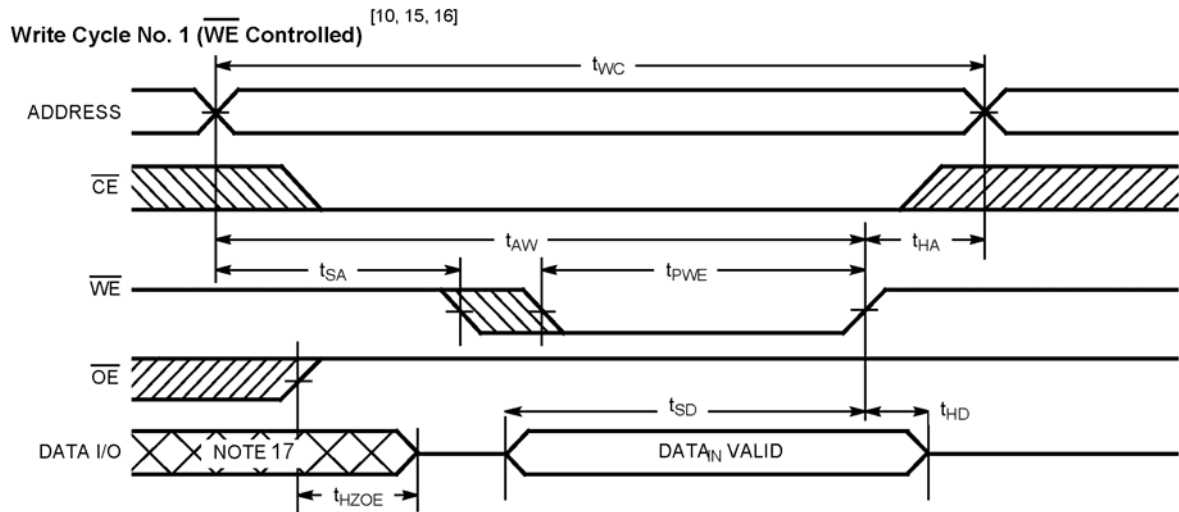
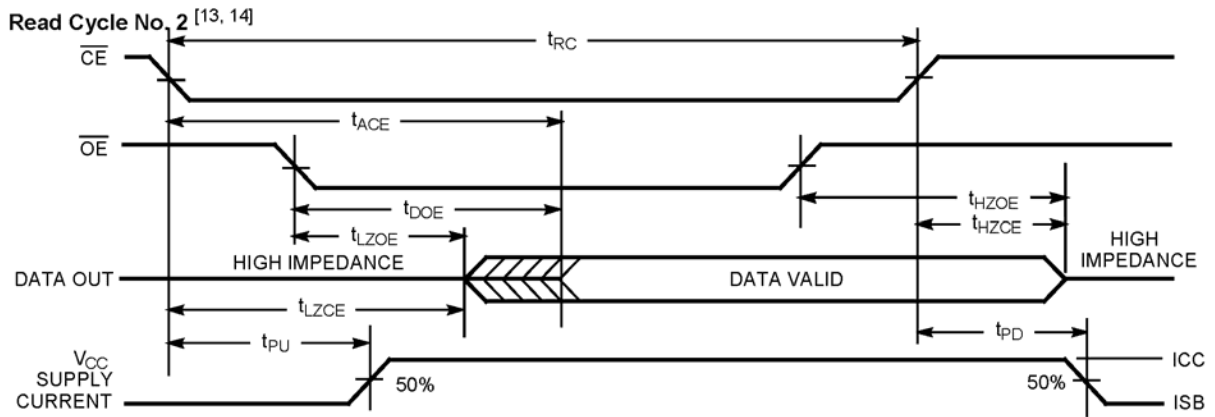
10. The internal Write time of the memory is defined by the overlap of $\overline{OE}$ LOW and $\overline{WE}$ LOW. Both signals must be Low to initiate a Write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the Write.

11. The minimum Write cycle time for Write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}

12. Device is continuously selected. $\overline{OE}$, $\overline{OE}=V_{IL}$.

13. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

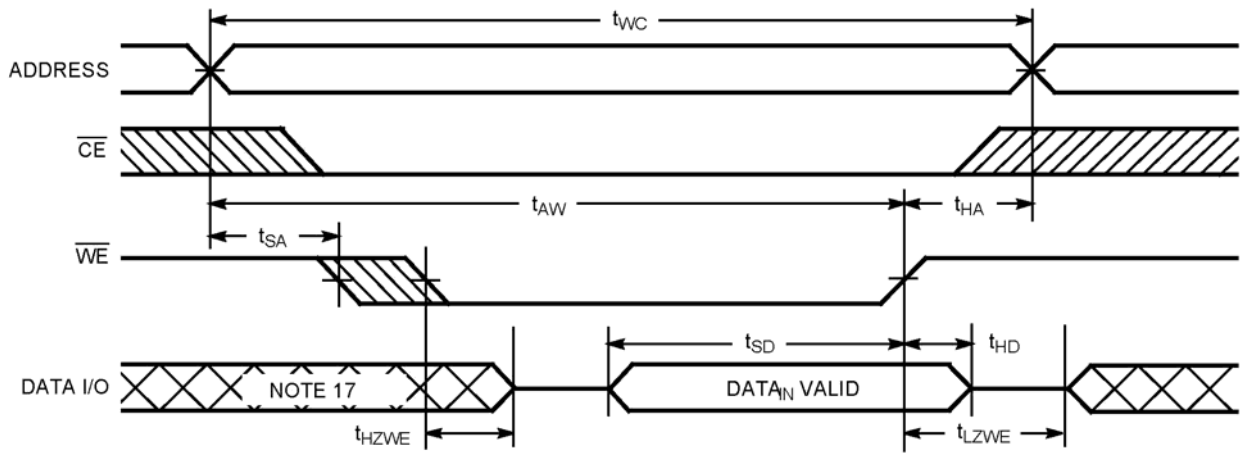


Notes:

14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

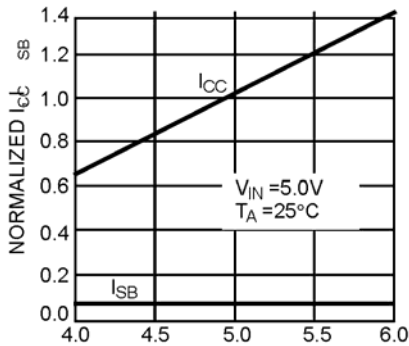
Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[11, 16]

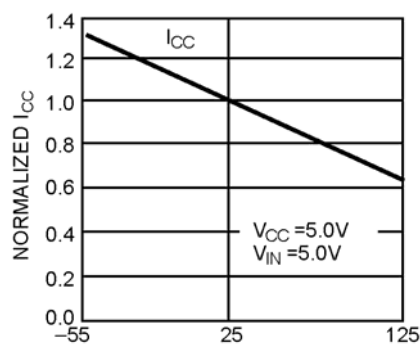


Typical DC and AC Characteristics

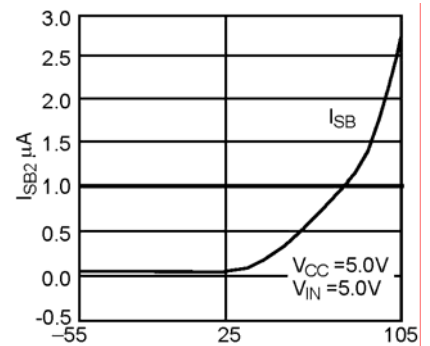
**NORMALIZED SUPPLY CURRENT
Vs. SUPPLY VOLTAGE**



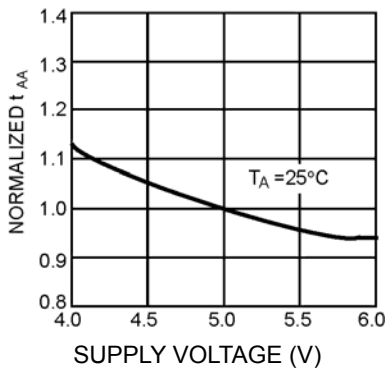
**NORMALIZED SUPPLY CURRENT
Vs. AMBIENT TEMPERATURE**



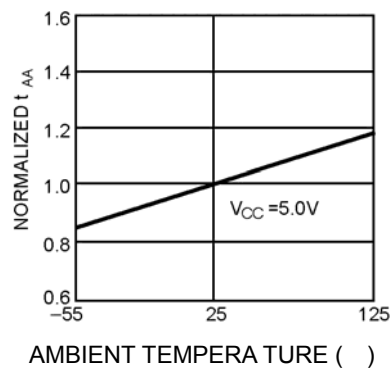
**STANDBY CURRENT
Vs. AMBIENT TEMPERATURE**



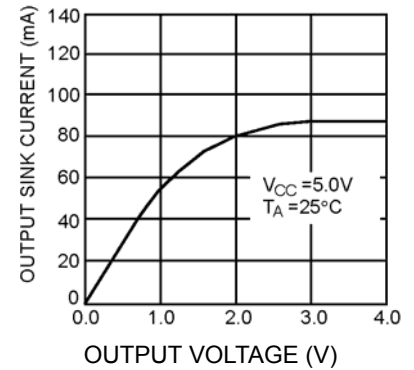
**NORMALIZED ACCESS TIME
Vs. SUPPLY VOLTAGE**



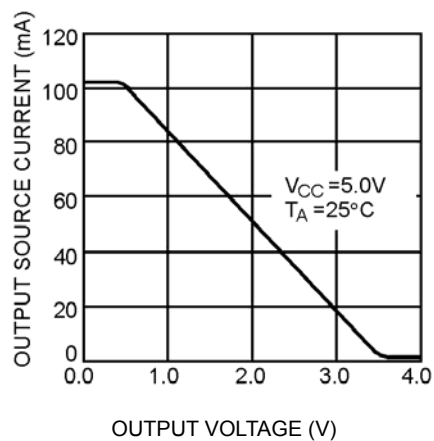
**NORMALIZED ACCESS TIME
Vs. AMBIENT TEMPERATURE**

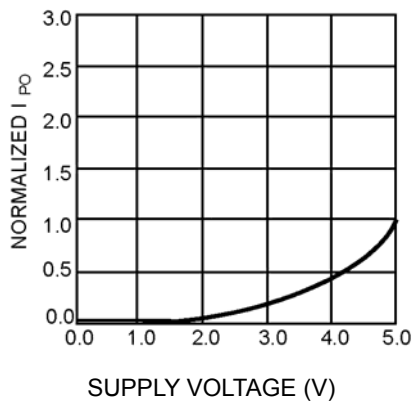
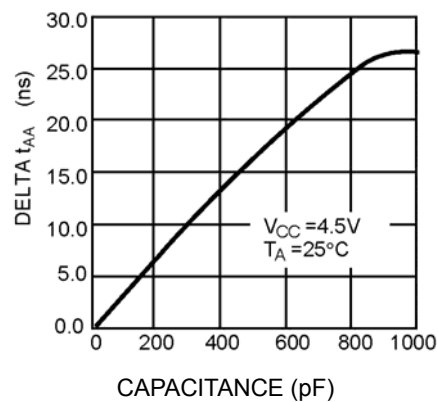
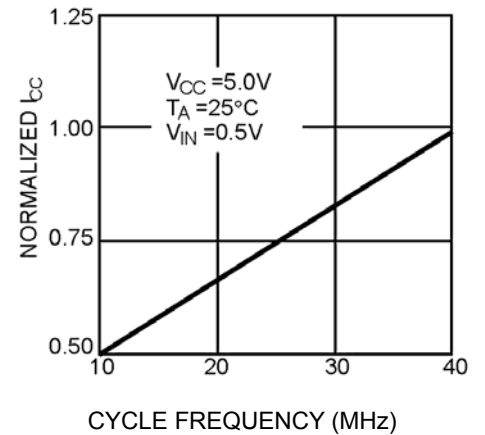


**OUTPUT SINK CURRENT
Vs. OUTPUT VOLTAGE**



**OUTPUT SOURCE CURRENT
Vs. OUTPUT VOLTAGE**



Typical DC and AC Characteristics (continued)
TYPICAL POWER-ON CURRENT
Vs. SUPPLY VOLTAGE

TYPICAL ACCESS TIME CHANGE
Vs. OUTPUT LOADING

NORMALIZED ICC vs. CYCLE TIME

Truth Table

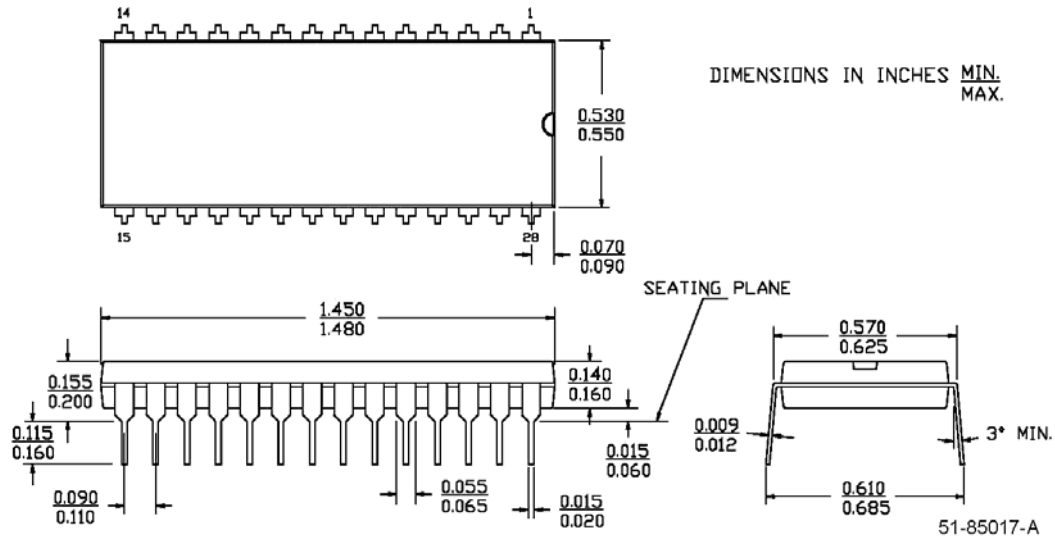
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Output Disabled	Active (I_{CC})

Ordering Information

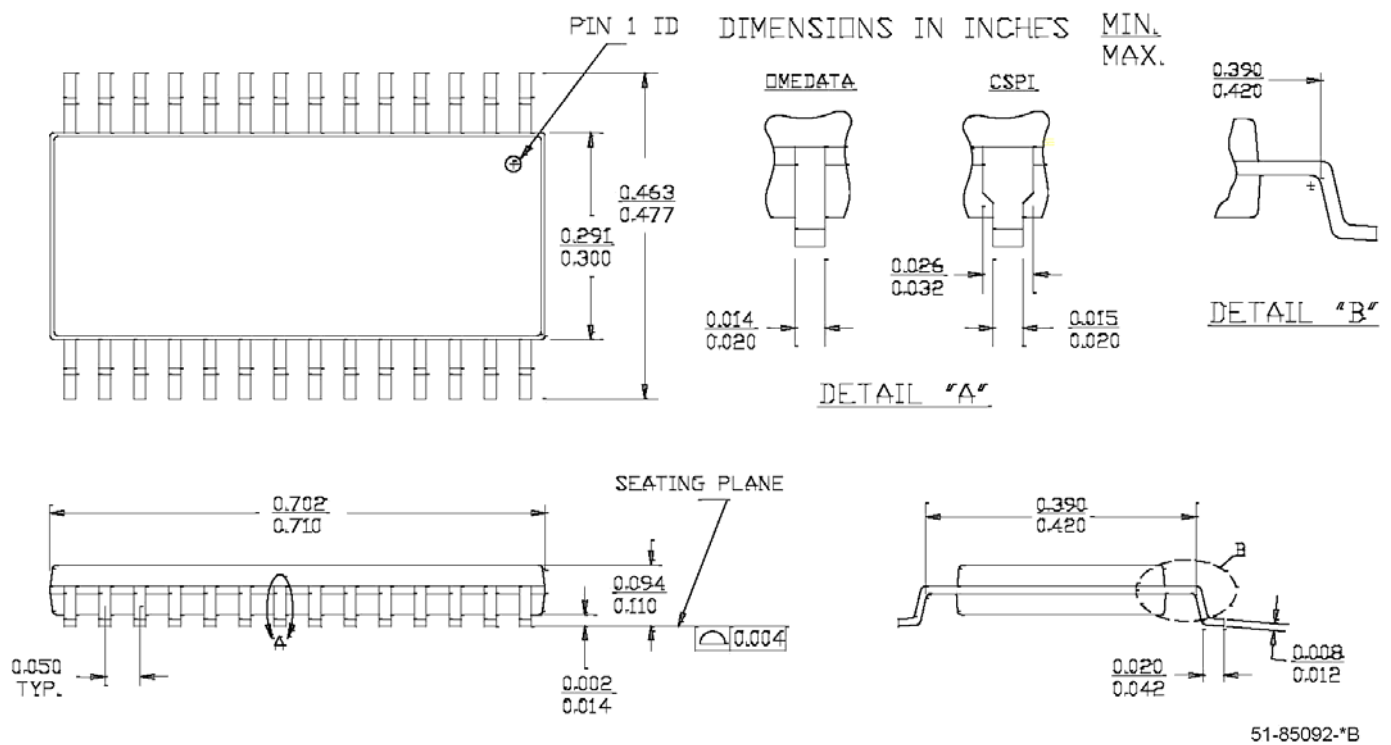
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62256LL-55SNI	SN28	28-lead (300-Mil Narrow Body) Narrow SOIC	Industrial
	CY62256LL-55ZI	Z28	28-lead Thin Small Outline Package	
	CY62256LL-55SNE	SN28	28-lead (300-Mil Narrow Body) Narrow SOIC	Automotive
	CY62256LL-55ZE	Z28	28-lead Thin Small Outline Package	
	CY62256LL-55ZRE	ZR28	28-lead Reverse Thin Small Outline Package	
70	CY62256-70SNC	SN28	28-lead (300-Mil Narrow Body) Narrow SOIC	Commercial
	CY62256L-70SNC			Industrial
	CY62256LL-70SNC			
	CY62256L-70SNI			
	CY62256LL-70SNI			
	CY62256LL-70ZC	Z28	28-lead Thin Small Outline Package	Commercial
	CY62256LL-70ZI	Z28		Industrial
	CY62256-70PC	P15	28-lead (600-Mil) Molded DIP	Commercial
	CY62256L-70PC	P15		
	CY62256LL-70PC	P15		
	CY62256LL-70ZRI	ZR28	28-lead Reverse Thin Small Outline Package	Industrial

Package Diagrams

28-lead (600-mil) Molded DIP P15



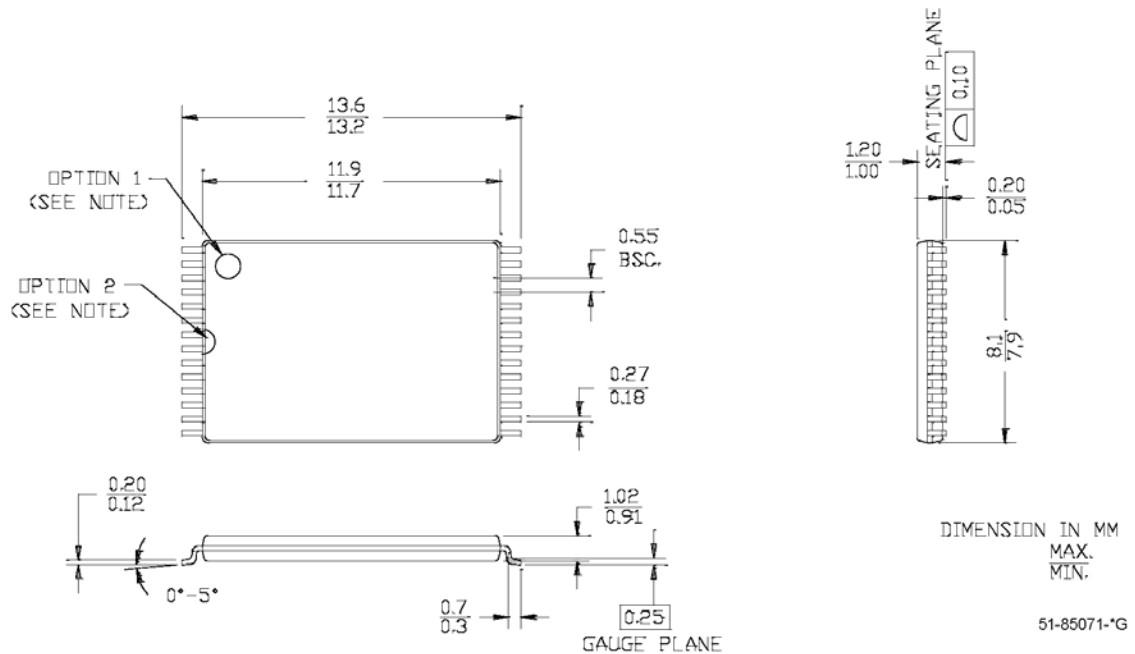
28-lead (300-mil) SNC (Narrow Body) SN28



Package Diagrams (continued)

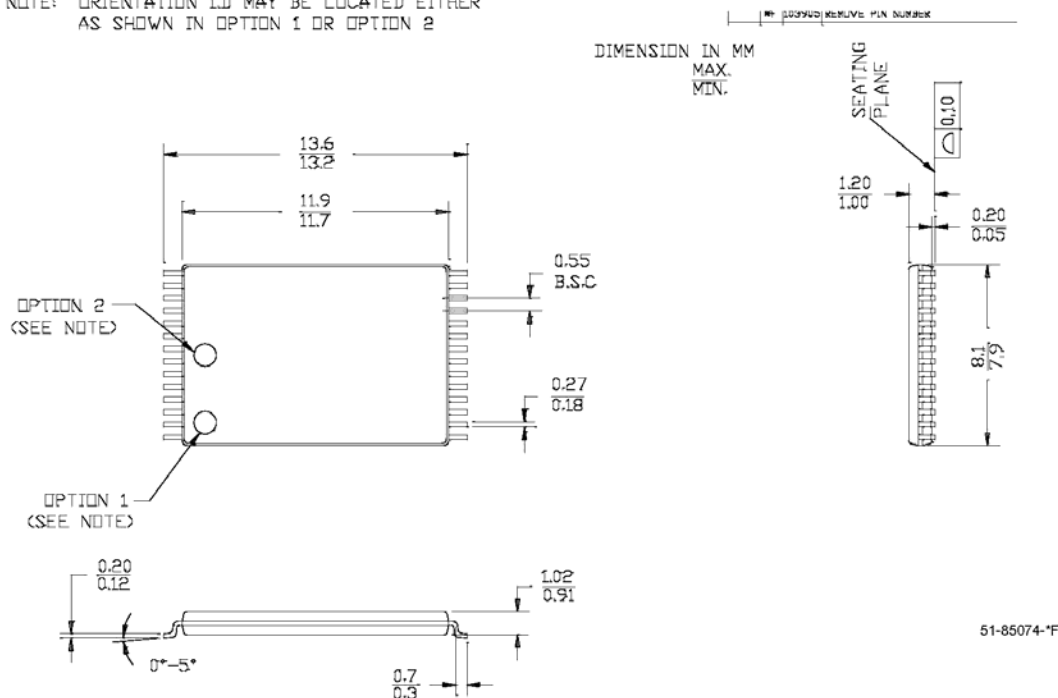
28-lead Thin Small Outline Package Type 1 (8 x 13.4 mm) Z28

NOTE: ORIENTATION ID MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2



28-lead Reverse Type 1 Thin Small Outline Package (8 x 13.4 mm) ZR28

NOTE: ORIENTATION ID MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2



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Document Title: CY62256 256K (32k x 8) Static RAM**Document Number: 38-05248**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113454	03/06/02	MGN	Change from Spec number: 38-00455 to 38-05248 Remove obsolete parts from ordering info, standardize format
*A	115227	05/23/02	GBI	Changed SN Package Diagram
*B	116506	09/04/02	GBI	Added footnote 1. Corrected package description in Ordering information table
*C	238448	See ECN	AJU	Added Automotive product information